

Abstract of the Disclosure

A computer system comprises a memory controller and a synchronous non-volatile memory device coupled to the memory controller via a main memory bus. The synchronous non-volatile memory device has external interconnects arranged in a manner that corresponds to interconnects of a synchronous dynamic random access memory device. The synchronous flash memory device, however, comprises a reset connection, and a Vccp power supply connection correspond to first and second no-connect (NC) interconnect pins of the synchronous dynamic random access memory. In one embodiment, the synchronous non-volatile memory device has a command interface comprising a write enable connection (WE#) to receive a write enable signal, a column address strobe connection (CAS#) to receive a column address strobe signal, a row address strobe connection (RAS#) to receive a row address strobe signal, and a chip select connection (CS#) to receive a chip select signal.

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